AMENDMENTS TO THE CLAIMS

1-11. (Canceled)

12. (Currently Amended) An input/output (I/O) device for use in a process control system for providing communications between a process controller and a first device ~~in a process control network~~, the process control system including a plurality of I/O devices in communication with the process controller using a bus, the I/O device comprising:

~~an~~ first interface for communicatively linking the I/O device with a process controller via the bus, the first interface adapted to receive signals from the process controller for the first device via the bus;

a second interface for communicatively linking the I/O device with the first device apart from the bus; and

a device processor coupled with the first interface for controlling operation of the I/O device including performing fault detection for the I/O device;

wherein the device processor, upon detection of a potential device fault, severs the communication link provided by the first interface with the bus.

13. (Currently Amended) The I/O device of claim 12 wherein the bus includes a data line and the first interface communicatively links the I/O device with the data line of the bus, and wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the first interface with the data line.

14. (Currently Amended) The I/O device of claim 13 wherein the I/O device further comprises a relay ~~device~~ coupled between the device processor and the data line of the bus, the relay having a first state communicatively linking the I/O device with the data line, and a second state severing the communicative link between the I/O device and the data line of the bus, wherein the device processor, upon detection of the potential device fault, severs the communication link with the bus by actuating the relay to the second state.

15. (Original) The I/O device of claim 13 wherein the data line of the bus is a data line capable of being affected by the I/O device.

16. (Previously Presented) The I/O device of claim 15 wherein the data line of the bus is at least one of a transmit data line and a clock data line.

17. (Currently Amended) The I/O device of claim 13 ~~and~~ further comprising a driver device coupled between the device processor and the first interface, the driver device having a driver output coupled to the interface and readable by the processor, wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the interface with the data line, performs further fault detection on the I/O device by forcing states to the driver output, and determines a device fault responsive to readings from the driver output.

18. (Currently Amended) The I/O device of claim 12 wherein the bus includes a plurality of data lines, and the first interface communicatively links the I/O device to the plurality of data lines, wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the first interface with the plurality of data lines of the bus.

19. (Original) The I/O device of claim 12 wherein the fault detection is an initial fault detection, and further comprising a later fault detection performed by the I/O device after the communicative link from the I/O device and the bus is severed.

20. (Original) The I/O device of claim 19 wherein the later fault detection is performed in a similar manner to the initial fault detection.

21. (Previously Presented) The I/O device of claim 12 wherein the potential device fault includes the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus, and the device processor severing of the communication link with the bus allows the other I/O devices to communicate to one another over the bus.

22. (Currently Amended) The I/O device of claim 21 wherein the bus includes at least one data line and the first interface communicatively links the I/O device with the at least one data line of the bus, and the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus includes the I/O device affecting the bus by the I/O device transmitting an undesired signal on the at least one data line of the bus, where the device processors severing of the communication link with the bus allows the other I/O devices to communicate to one another over the bus.

23. (Currently Amended) The I/O device of claim 12 wherein the device processor[[s]] fault detection includes the device processor attempting to affect the bus using the first interface, wherein the device processor detects the potential device fault by an inability of the device processor to affect the bus.

24. (Original) The I/O device of claim 23 wherein the device processor attempting to affect the bus includes the device processor attempting to change the state of the bus.

25. (Original) The I/O device of claim 24 wherein the device processor attempting to change the state of the bus includes the device processor forcing a state on the bus.

26. (Original) The I/O device of claim 25 wherein the device processor forcing the state of the bus includes the device processor transmitting one of a digital high value and a digital low value on the bus.

27. (Original) The I/O device of claim 23 further comprising the device processor reading the bus after attempting to affect the bus, wherein the device processor determines the inability to affect the bus using the reading of the bus.

28. (Previously Presented) The I/O device of claim 12 further comprising the device processor performing further fault detection upon severing of the communication link, wherein when the device processor detects no device fault from the further fault detection, the device processor reestablishes the communication link with the bus.

29. (Original) The I/O device of claim 12 wherein the process control system operates in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising the I/O device being assigned to one of the synchronous time slots, where the device processor performs fault detection during the asynchronous time slot following the corresponding synchronous time slot.

30. (Original) The I/O device of claim 12 wherein the device processor performs the fault detection when the I/O device is not transmitting I/O device information on the bus.

31-36. (Canceled)

37. (Withdrawn) A process control system for communications in a process control network having a plurality of devices in communication using a bus, the process control system comprising:

a primary redundant device communicatively linked to the bus; and

a secondary redundant device communicatively linked to the bus, and programmed to detect a primary redundant device fault;

wherein, the secondary redundant device, upon detecting the primary redundant device fault, publishes a primary redundant device fault message on the bus.

38. (Withdrawn) The process control system of claim 37 further comprising a controller communicatively linked to the bus and including a controller processor programmed to process messages published on the bus, wherein the controller deactivates the primary redundant device responsive to the primary redundant device fault message.

39. (Withdrawn) The process control system of claim 38 further comprising the controller activating the secondary redundant device.

40. (Withdrawn) The process control system of claim 38 wherein the primary redundant device is further programmed to perform fault detection, and further comprising a primary fault detect order message published by the controller causing the primary redundant device to perform fault detection.

41. (Withdrawn) The process control system of claim 40 wherein the secondary redundant device is capable of detecting secondary redundant device faults, and further comprising:

a primary redundant device no fault message published on the bus to the controller where no fault is detected in the primary redundant device; and

a secondary fault detect order message published by the controller responsive to the primary redundant device no fault message causing the secondary redundant device to perform fault detection.

42. (Withdrawn) The process control system of claim 37 wherein the primary redundant device is further programmed to perform fault detection, and responsive to the

primary redundant device fault message, the primary redundancy device performs fault detection.

43. (Withdrawn) The process control system of claim 37 further comprising a direct communication link between the primary redundant device and the secondary redundant device, wherein the secondary redundant device detects the primary redundant device fault using the direct communication link.

44. (Withdrawn) The process control system of claim 43 wherein the secondary redundant device detects the primary redundant device fault based on information received over the direct communication link.

45. (Withdrawn) A method of configuring an input/output (I/O) device for use in a process control system, the process control system having a controller operating under a particular version of I/O communication software, the method comprising:

storing a plurality of versions of I/O communication software in a storage device for the I/O device, each version of I/O communication software usable by a device processor of the I/O device in controlling the I/O device;

determining by the device processor the particular version of I/O communication software utilized by the controller;

determining by the device processor a version of I/O communication software of the plurality of versions of I/O communication software stored in the storage device that is compatible with the particular version of communication protocol used by the controller; and

configuring the I/O device to operate using the compatible version of I/O communication software.

46. (Withdrawn) The method of claim 45 wherein the controller transmits a message to the I/O device, and further comprising generating a responsive message at the device processor including information regarding the versions of I/O communication software stored in the storage device of the I/O device.

47. (Withdrawn) The method of claim 46 wherein the version of I/O communication software comprises a plurality of versions including a primitive version and at least one less primitive version, and the generating a responsive message includes generating a first message portion utilized in the primitive version and the less primitive version of the I/O communication software, and generating a second portion utilized only in the less primitive version of the I/O communication software, and placing the information regarding the version of the I/O communication software stored in the storage device in the second message portion.

48. (Withdrawn) The method of claim 47 wherein the message generated by the controller is a first message, and further comprising:

generating a second message by the controller including a first message portion utilized in the primitive version and the less primitive version of the I/O communication software, and a second portion utilized only in the less primitive version of the I/O communication software;

placing information by the controller in the second portion of the second message when the controller uses a less primitive version of the I/O communication software, and

leaving the second portion of the second message unused when the controller utilizes the primitive version of the I/O communication software;

sending the second message from the controller to the I/O device; and

determining by the device processor the particular version of I/O communication software utilized by the controller responsive to information placed in the second portion of the second message.

49. (Withdrawn) The method of claim 45 further comprising:

generating an identification message at the controller including information regarding the version of I/O communication software utilized by the controller; and

sending the identification message from the controller to the I/O device;

wherein the determining of a version of I/O communication software includes extracting the version information from the identification message by the device processor, and determining the particular version of I/O communication software utilized by the controller using the version information.

50. (Withdrawn) The method of claim 49 further comprising generating by the device processor a reply identification message responsive to the identification message identifying the versions of the I/O communication software stored in the storage device.

51. (Withdrawn) The method of claim 45 wherein the determining of the compatible version of I/O communication software includes determining at the device processor the same version of I/O communication software as the particular version of I/O communication software utilized by the controller.

52. (Withdrawn) The method of claim 45 wherein the determining of the compatible version of I/O communication software includes determining at the device processor a more primitive version of I/O communication software than the particular version of I/O communication software utilized by the controller.

53. (Withdrawn) The method of claim 45 wherein the I/O device is communicatively linked to at least one field device, and further comprising communicating with the at least one field device using a Fieldbus communication protocol.

54. (Withdrawn) The method of claim 45 wherein the I/O device is communicatively linked to at least one field device, and further comprising communicating with the at least one field device using a HART communication protocol.

55. (Canceled)

56. (Currently Amended) A method for severing communication between an input/output (I/O) device and a bus in a process control system, the process control system including a plurality of I/O devices communicatively linked with a process controller using ~~a~~ the bus, the method comprising:

providing ~~an~~ first interface for communicatively linking the I/O device with a process controller via the bus, the first interface adapted to receive signals from the process controller for the first device via the bus;

providing a second interface for communicatively linking the I/O device with the first device apart from the bus;

performing fault detection by a device processor of the I/O device; and

severing the communication link provided by the first interface when the device processor detects a potential device fault in the I/O device.

57. (Currently Amended) The method of claim 56 wherein the bus includes a data line, and:

providing the first interface includes providing the first interface for communicatively linking the I/O device with the data line; and

~~the~~ severing of the communication link includes severing the communication link provided by the first interface with the data line when the device processor detects a potential device fault in the I/O device.

58. (Currently Amended) The method of claim 57 ~~wherein the I/O device~~ further comprising[[es]]:

providing a relay device between the device processor and the first interface, the relay communicatively linking the I/O device with the data line in a first state, and severing the communicative link between the I/O device and the data line of the bus in a second state;

wherein the severing of the communication link provided by the first interface includes actuating the relay to the second state by the device processor.

59. (Currently Amended) The method of claim 57 wherein ~~the~~ severing of the communication link provided by the first interface with the data line includes severing the communication link provided by the first interface with a data line capable of being affected by the I/O device.

60. (Currently Amended) The method of claim 59 wherein ~~the~~ severing of the communication link provided by the first interface with the data line includes severing the communication link provided by the first interface with at least one of a transmit data line and clock data line.

61. (Currently Amended) The method of claim 57 ~~and~~ further comprising:

providing a driver device between the device processor and the first interface, the device driver having a driver output coupled to the first interface and the device processor; and

performing further fault detection on the I/O device by forcing states to the driver output and reading the state of the driver output by the device processor upon severing the communication link with the first interface;

wherein determining of the device fault includes determining of the device fault responsive to the reading of the state of the driver output.

62. (Currently Amended) The method of claim 56 wherein the bus includes a plurality of data lines, and further including;

providing the first interface includes providing the first interface communicatively linking the I/O device to the plurality of data lines,

wherein the severing of the communication link includes severing the communication link provided by the first interface to the plurality of data lines of the bus upon detection of a device fault.

63. (Previously Presented) The method of claim 56 wherein the fault detection is an initial fault detection, and further comprising:

performing a later fault detection by the I/O device after the communicative link from the I/O device and the bus is severed.

64. (Original) The method of claim 63 wherein the performing the later fault detection includes performing the later fault detection in a similar manner as the initial fault detection.

65. (Original) The method of claim 63 further comprising reestablishing the communication link with the bus by the device processor when the later fault detection detects no I/O device fault.

66. (Original) The method of claim 56 wherein the performing the fault detection includes attempting to affect the bus using the communicating link, wherein the potential device fault is detected by an inability to affect the bus.

67. (Original) The method of claim 66 wherein the attempting to affect the bus includes attempting to change the state of the bus.

68. (Original) The method of claim 67 wherein the attempting to change the state of the bus includes forcing a state on the bus.

69. (Original) The method of claim 68 wherein the forcing the state of the bus includes forcing the bus to one of a digital high value and a digital low value.

70. (Original) The method of claim 56 wherein the process control system operates in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising assigning the I/O device to one of the synchronous time slots, wherein the performing of the fault detection by the device processor includes performing the fault detection during the asynchronous time slot following the corresponding synchronous time slot which the I/O device is assigned.

71. (Original) The method of claim 56 wherein the performing of the fault detection by the device processor includes performing the fault detection when the I/O device is not transmitting I/O device information on the bus.

72-79. (Canceled)

80. (Currently Amended) An apparatus for use in a process control system, the process control system including a plurality of devices in communication using a bus, the apparatus being one of an input/output (I/O) device and a field device and comprising:

an interface for communicatively linking the apparatus with a process controller via the bus, the first interface adapted to receive signals from the process controller for a first device via the bus, the first device being coupled to the apparatus through a second interface apart from the bus;

a processor coupled with the interface for controlling operation of the apparatus including performing fault detection for the apparatus;

wherein the processor, upon detection of a potential apparatus fault, severs the communication link provided by the interface with the bus.

81-86. (Canceled)

87. (Previously Presented) The apparatus of claim 80 wherein the apparatus is an input/output (I/O) device.

88. (Currently Amended) The apparatus of claim 87 wherein the bus includes a data line and the first interface communicatively links the apparatus with the data line of the bus, and wherein the processor, upon detection of the potential apparatus fault, severs the communication link provided by the first interface with the data line.

89. (Previously Presented) The apparatus of claim 88 wherein the apparatus further comprises a relay coupled between the processor and the data line of the bus, the relay having a first state communicatively linking the apparatus with the data line, and a second state severing the communicative link between the apparatus and the data line of the bus, wherein the processor, upon detection of the potential apparatus fault, severs the communication link with the bus by actuating the relay to the second state.

90. (Previously Presented) The apparatus of claim 88 wherein the data line of the bus is a data line capable of being affected by the apparatus.

91. (New) A process control system, comprising:

a bus;

a process controller communicatively coupled to the bus; and

a plurality of I/O devices coupled to the bus for providing communications between the process controller and a plurality of first devices, wherein each I/O device includes;

a first interface for communicatively linking the I/O device to the bus; and

a device processor coupled with the first interface for controlling operation of the I/O device including performing fault detection for the I/O device, and, upon detection of a potential I/O device fault, severing the communication link provided by the first interface with the bus.

92. (New) The system of claim 91 wherein each I/O device of the plurality of I/O devices further comprises a second interface for coupling the I/O device to at least one of the plurality of first devices.

93. (New) The system of claim 92 wherein the at least one of the plurality of first devices is a field device.

94. (New) The system of claim 91 wherein the bus includes a data line and the first interface of each I/O device communicatively links the I/O device with the data line of the bus, and wherein the device processor of each I/O device, upon detection of the potential device fault, severs the communication link provided by the first interface of the I/O device with the data line.

95. (New) The system of claim 94 wherein each I/O device further comprises a relay coupled between the device processor of each I/O device and the data line of the bus, the relay having a first state communicatively linking the I/O device with the data line, and a second state severing the communicative link between the I/O device and the data line of the

bus, wherein the device processor, upon detection of the potential device fault, severs the communication link with the bus by actuating the relay to the second state.

96. (New) The system of claim 94 wherein the data line of the bus is a data line capable of being affected by each of the plurality of I/O devices.

97. (New) The system of claim 96 wherein the data line of the bus is at least one of a transmit data line for transmitting first device information from each of the plurality of I/O devices to the controller, and a clock data line.

98. (New) The system of claim 94 wherein each of the plurality of I/O devices further comprises a driver device coupled between the device processor and the first interface, the driver device having a driver output coupled to the first interface and readable by the processor, wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the interface with the data line, performs further fault detection on the I/O device by forcing states to the driver output, and determines a device fault responsive to readings from the driver output.

99. (New) The system of claim 91 wherein the bus includes a plurality of data lines, and the first interface of each of the plurality of I/O devices communicatively links the I/O device to the plurality of data lines, wherein the device processor of the I/O device, upon detection of the potential device fault, severs the communication link provided by the first interface with the plurality of data lines of the bus.

100. (New) The system of claim 91 wherein the fault detection is an initial fault detection, and further comprises a later fault detection performed by the I/O device after the communicative link from the I/O device and the bus is severed.

101. (New) The system of claim 100 wherein the later fault detection is performed in a similar manner to the initial fault detection.

102. (New) The system of claim 91 wherein the potential device fault includes one of the plurality of I/O devices prohibiting another of the plurality of I/O devices utilizing the bus from communicating over the bus, and the device processor of the one of the I/O devices severing the communication link with the bus allows the other I/O devices to communicate over the bus.

103. (New) The system of claim 91 wherein the fault detection of one of the device processors of the plurality of I/O devices includes the device processor of the one of the plurality of I/O devices attempting to affect the bus using the first interface of the one of the device processors, wherein the device processor of the one of the plurality of I/O devices detects the potential device fault by an inability of the device processor of the one of the I/O devices to affect the bus.

104. (New) The system of claim 103 wherein the device processor for one of the plurality of I/O devices attempting to affect the bus includes the device processor for the one of the plurality of I/O devices attempting to change the state of the bus.

105. (New) The system of claim 104 wherein the device processor for one of the plurality of I/O devices attempting to change the state of the bus includes the device processor for the one of the plurality of I/O devices forcing a state on the bus.

106. (New) The system of claim 105 wherein the device processor for one of the plurality of I/O devices forcing the state of the bus includes the device processor for the one of the plurality of I/O devices transmitting one of a digital high value and a digital low value on the bus.

107. (New) The system of claim 105 further comprising the device processor for one of the plurality of I/O devices reading the bus after attempting to affect the bus, wherein the device processor for the one of the plurality of I/O devices determines the inability to affect the bus using the reading of the bus.

108. (New) The system of claim 91 further comprising the device processor for one of the plurality of I/O devices performing further fault detection upon severing of the communication link, wherein when the device processor for the one of the plurality of I/O devices detects no device fault from the further fault detection, the device processor for the one of the plurality of I/O devices reestablishes the communication link with the bus.

109. (New) The system of claim 91 wherein the process control system operates in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising one of the plurality of I/O devices being assigned to one of the synchronous time slots, where the device processor for the one of the plurality of I/O devices performs fault detection during the asynchronous time slot following the corresponding synchronous time slot.

110. (New) The system of claim 91 wherein the device processor of one of the plurality of I/O devices performs the fault detection when the one I/O device of the plurality of I/O devices is not transmitting I/O device information on the bus.